# EXHIBIT A

**EXHIBIT A - JOINT CLAIM CONSTRUCTION STATEMENT**
***Netlist, Inc. v. Micron Technology, Inc., et al.*, No. 1:22-cv-00134-LY**
***Netlist, Inc. v. Micron Technology, Inc., et al.*, No. 1:22-cv-00136-LY**

## I. Terms to Be Jointly Construed with *Netlist, Inc. v. Micron Technology, Inc., et al.*, No. 1:22-cv-00134-LY

### A. U.S. Patent No. 8,301,833 ("'833 Patent")

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| 1. "volatile memory subsystem" / "non-volatile memory subsystem" ('833 Pat., Cl. 15) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. | '833 Patent<br>• 7:8-11<br>• 18:14-29<br>• 18:33-44<br>• Fig. 1<br>• Fig. 4A<br><br>Declaration of Steven Przybylski, Ph. D. | "volatile memory subsystem" means "one or more volatile memory devices."<br><br>"non-volatile memory subsystem" means "one or more non-volatile memory devices." | '833 Patent<br>• 4:57-61<br>• 5:48-6:36<br>• 7:66-8:56<br>• 10:43-58<br>• 12:53-55<br>• 13:57-14:47<br>• 15:59-16:37<br>• 17:18-21<br>• 18:22-50<br>• 19:20-26<br>• 20:14-61<br>• Fig. 1<br>• Fig. 2<br>• Fig. 3<br>• Fig. 8<br><br>*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper 7 (Patent Owner Preliminary Response) (Opening Br., Ex. 14) at p. 12. |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | | | | *SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper 8 (Trial Institution Decision) (Opening Br., Ex. 15) at p. 12.<br><br>*SMART Modular Tech., Inc. v. Netlist, Inc.*, IPR2014-01370, Paper 11 (Patent Owner Preliminary Response) (Opening Br., Ex. 16) at pp. 11-12.<br><br>*SMART Modular Tech., Inc. v. Netlist, Inc.*, IPR2014-01370, Paper 13 (Trial Institution Decision) (Opening Br., Ex. 17) at p. 16.<br><br>*SK hynix Inc. et al. v. Netlist*, Inc., IPR2017-00649, Paper 6 (Patent Owner Preliminary Response) (Opening Br., Ex. 18) at p. 4. |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| 2. "controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation" ('833 Pat., Cl. 16) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.<br><br>Not subject to § 112, ¶ 6. | '833 Patent<br>• 2:46-49<br>• 2:51-59<br>• 4:58-61<br>• 4:63-64<br>• 6:54-59<br>• 6:63-7:40<br>• 8:22-36<br>• 10:8-22<br>• 10:55-58<br>• 15:46-16:3<br>• 22:12-17<br><br>Declaration of Steven Przybylski, Ph. D. | This is a means-plus-function limitation.<br><br>Function: entire limitation after "*configured to*."<br><br>Corresponding Structure: "controller that is separate from the volatile and non-volatile memory subsystems," as described in the '833 Patent, 6:63-7:40. | '833 Patent<br>• Abstract<br>• 3:62-64<br>• 4:57-61<br>• 6:54-7:40<br>• 7:66-8:56<br>• 10:19-22<br>• 13:57-14:47<br>• 15:59-16:37<br>• 18:29-20:61<br>• Fig. 1<br>• Fig. 2<br>• Fig. 3<br>• Fig. 8<br><br>*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper 8 (Trial Institution Decision) (Opening Br., Ex. 15) at p. 12.<br><br>Declaration of Harold S. Stone, Ph. D. |

## II. Terms to Be Jointly Construed with *Netlist, Inc. v. Micron Technology, Inc., et al.*, No. 1:22-cv-00136-LY

### A. U.S. Patent Nos. 9,824,035 and 10,268,608 ("Lee Patents")

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| 1. "module control device" ('035 & '605 Pats., Cl. 1) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.<br><br>Neither indefinite nor subject to § 112, ¶ 6. | '035 Patent<br>• 1:40-2:35<br>• 4:18-43<br>• 4:63-5:8<br>• 5:55-67<br>• 8:6-30<br>• 9:49-54<br>• Figs. 1, 2A, 2B, 2C, 2D, 7, 12A, 12B<br><br>'608 Patent<br>• 1:43-2:36<br>• 4:20-35<br>• 4:65-5:10<br>• 5:58-6:3<br>• 8:9-34<br>• 9:52-57<br>• Figs. 1, 2A, 2B, 2C, 2D, 7, 12A, 12B<br><br>Declaration of Steven Przybylski, Ph. D. | This is a means-plus-function limitation.<br><br>Function: entire limitation after "configured to."<br><br>Corresponding Structure: Indefinite – no corresponding structure | Declaration of Alan Jay Smith, Ph. D. (No intrinsic evidence because no corresponding structure) |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| 2. "logic"<br>('035 Pat., Cl. 1) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.<br><br>Neither indefinite nor subject to § 112, ¶ 6. | '035 Patent<br>• 4:18-33<br>• 5:40-54<br>• 8:1-5<br>• 8:18-30<br>• 9:27-29<br>• 9:33-35<br>• 9:42-48<br>• 10:8-18<br>• 10:47-66<br>• 11:5-15<br>• 11:66-17:49<br>• 18:9-15<br>• 18:63-19:7<br>• Figs. 3, 6, 8-19<br><br>Declaration of Steven Przybylski, Ph. D.<br><br>Wiley Electrical and Electronics Engineering Dictionary (2004) (Ex. E to Przybylski Decl.). | This is a means-plus-function limitation.<br><br>Function: entire limitation after "configured to." In addition, the entire limitation after "the logic is further configured to."<br><br>Corresponding Structure: Indefinite – no corresponding structure | Declaration of Alan Jay Smith, Ph. D. (No intrinsic evidence because no corresponding structure)<br><br>'035 Patent<br>• 13:44-48<br>• 14:60-65 |
| 3. "command processing circuit"<br>('608 Pat., Cl. 1) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire | '608 Patent<br>• 4:65-5:4<br>• 5:43-57<br>• 10:50-11:7<br>• 12:11-26 | This is a means-plus-function limitation.<br><br>Function: entire limitation after | Declaration of Alan Jay Smith, Ph. D. (No intrinsic evidence because no corresponding structure) |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | disclosure.<br><br>Neither indefinite nor subject to § 112, ¶ 6. | • 14:57-17:54<br>• 18:14-20<br>• 19:1-12<br>• Figs. 3, 6, 7, 11A, 11B, 12A, 12B, 14-16, 19<br><br>Declaration of Steven Przybylski, Ph. D. | "configured to" and before "and a delay circuit."<br><br>Corresponding Structure: Indefinite – no corresponding structure | |

**B. U.S. Patent No. 10,489,314 ("'314 Patent")**

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| 1. "burst of data strobes" ('314 Pat., Cls. 1, 15, 25, 28) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Not indefinite.<br><br>In the alternative "strobe signals with successive rising and falling edges, each edge | '314 Patent<br>• 3:17-4:30<br>• 5:36<br>• 6:39-43<br>• 7:28-48<br>• 13:18-51<br>• 13:60-14:22<br>• 14:41-56<br>• 22:59<br>• 23:27<br>• 23:67<br>• 26:9<br>• 31:35 | Indefinite. | '314 Patent<br>• 13:18-23<br>• Fig. 1<br>• Fig. 6A<br>• Fig. 6B<br>• Fig. 7<br>• Fig. 18<br>• Fig. 19<br><br>Declaration of Harold S. Stone, Ph. D. |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | being associated with one or more data bits." | • 35:20-23<br>• Figs. 2, 6A, 6B, 7<br><br>Declaration of Steven Przybylski, Ph. D.<br><br>JESD79-2A (Ex. B to Przybylski Decl.)<br>• pp. 26, 29, 30<br><br>JESD79-2B (Ex. C to Przybylski Decl.)<br>• pp. 26, 29, 92-103 | | |
| 2. "logic" terms ('314 Pat., Cls. 1, 15, 25) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.<br><br>Neither indefinite nor subject to § 112, ¶ 6. | <u>'314 Patent</u><br>• claims 1, 3, 15, 28<br>• 5:64-67<br>• 7:5-24<br>• 9:25-51<br>• 10:47-52<br>• 11:9-25<br>• 11:55-13:14<br>• 15:19-24<br>• 16:36-39<br>• 16:60-63<br>• 17:20-28<br>• 17:50-55 | This is a means-plus-function limitation.<br><br><u>Function</u><br>• For claim 1, "respond[ing] to the first/second memory command by providing first/second control signals to the circuitry" | Declaration of Harold S. Stone, Ph. D. (No intrinsic evidence because no corresponding structure) |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | | • 22:51-53<br>• 23:19-23<br>• 25:4-6<br>• 25:15-31:30<br>• 34:42-67<br>• Verilog examples 1-3<br>• Figs. 5A-5D, 9A-9B<br><br>Declaration of Steven Przybylski, Ph. D.<br><br>Wiley Electrical and Electronics Engineering Dictionary (2004) (Ex. E to Przybylski Decl.). | • For claims 15/25, "output[ting] first/second control signals to the circuitry . . . in response to the first/second read or write memory command"<br><br>Corresponding Structure: Indefinite – no corresponding structure. | |
| 3. "overall CAS latency . . ." / "actual operational CAS latency . . ." ('314 Pat., Cls. 1, 15, 25, 28) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.<br><br><u>In the alternative</u><br><br>"overall CAS latency of the memory module" | <u>'314 Patent</u><br>• Columns 10-13, 25-29, 30-32<br>• 7:20-26<br>• 9:34-42<br>• 10:47-52<br>• 15:26-33<br>• 22:28-63<br>• 25:25<br>• 25:44-27:8<br>• 29:16-20 | "overall CAS latency of the memory module" means "the delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module" | <u>'314 Patent</u><br>• 22:58-62<br><br>*Double Data Rate (DDR) SDRAM Specification*, Standard No. 79, JEDEC Solid State Tech. Corp. (June 2000) (Opening Br., Ex. 11) at pp. 10-11. |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | means "the delay between: (1) the time when a command is sampled on the memory module, and (2) a time when the first piece of data is available at the data pins of the memory module"<br><br>"actual operational CAS latency of each of the memory devices[/of each of the plurality of memory integrated circuits]" means "the delay between: (1) the time when a command is executed by each of the memory devices[/each of the plurality of memory integrated circuits], and (2) a time when the first piece of data is available at the data pins of each of the memory devices[/of each of the plurality of memory integrated circuits]" | • 31:34-40<br>• 36:36-38<br>• 44:49-50<br>• 45:14<br>• 45:19-20<br>• Verilog examples 1-3<br>• Figs. 3A-5D<br><br>Declaration of Steven Przybylski, Ph. D.<br><br>JESD79-2A (Ex. B to Przybylski Decl.)<br>• pp. 12, 24, 26<br><br>Synchronous DRAM Architectures, Organizations, and Alternative Technologies, by Prof. Bruce L. Jacob, dated December 10, 2002 ("Jacob Article") (Ex. D to Przybylski Decl.)<br>• p. 16<br><br>JESD79-2B (Ex. C to Przybylski Decl.)<br>• pp. 11-12, 24 | "actual operational CAS latency of each of the memory devices[/of each of the plurality of memory integrated circuits]" means "the delay between: (1) the time when a read command is executed by each of the memory devices[/each of the plurality of memory integrated circuits], and (2) the time when the first piece of data is made available at an output of each of the memory devices[/of each of the plurality of memory integrated circuits]" | *DDR SDRAM Registered DIMM Design Specification*, Standard No. 21-C, JEDEC Solid State Tech. Corp. (Rev. 1.3, Jan. 2002) (Opening Br., Ex. 12) at p. 68.<br><br>Declaration of Harold S. Stone, Ph. D. |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| 4. "circuitry" terms ('314 Pat., Cls. 1, 15, 25, 28) | Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.<br><br>Neither indefinite nor subject to § 112, ¶ 6. | '314 Patent<br>• 5:53-67<br>• 7:20-27<br>• 9:31-51<br>• 19:36-50<br>• 22:38-63<br>• 32:33-38<br>• Figs. 5A, 9A-9B, 10A-10B, 11A-11B<br>• Verilog examples 1-3 | This is a means-plus-function limitation.<br><br>The identified "circuitry" features in claims 1, 15, 25, and 28 are indefinite.<br><br>For claim 1, the "circuitry" feature is subject to § 112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the functions of:<br>(i) enabl[ing] data transfers through the circuitry in response to the first control signals;<br>(ii) enabl[ing] data transfers through the circuitry . . . subsequently in response to the second control signals; and<br>(iii) add[ing] a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS | Declaration of Harold S. Stone, Ph. D. (No intrinsic evidence because no corresponding structure) |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | | | latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.<br><br>The "circuitry" feature in claim 15 is subject to § 112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the functions of:<br>(i) enabl[ing] data transfers between the first rank and the memory bus through the circuitry in response to the first control signals; and<br>(ii) add[ing] a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency | |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | | | of each of the memory devices.<br><br>The additional "circuitry" feature in claim 25 is subject to § 112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: enabl[ing] registered data transfers between the second rank and the memory bus through the circuitry in response to the second control signals.<br><br>The "circuitry" feature in claim 28 is subject to § 112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the functions of: (i) add[ing] a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such | |

| Claim Term | Plaintiff's Proposed Construction | Plaintiff's Supporting Evidence | Defendants' Proposed Construction | Defendants' Supporting Evidence |
|---|---|---|---|---|
| | | | that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices; and (ii) the circuitry [of claim 28] includ[ing] logic pipelines configured to enable data transfers between the first rank and the memory bus in response to the first read or write memory command. | |